



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Application of :
Hirofumi HARADA :
Serial No. 09/872,798 : Group Art Unit: 2814
Filed: June 1, 2001 : Examiner: Thao X. Le
For: VERTICAL MOS TRANSISTOR :
AND A METHOD OF :
MANUFACTURING THE SAME : Docket No. S004-4310

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COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, DC 20231

RESPONSE

S I R:

In response to the Office Action dated April 22, 2002, applicant amends his application as follows:

IN THE SPECIFICATION:

Please replace the paragraph beginning at page 1, line 6, with the following rewritten paragraph:

--Fig. 2 illustrates a schematic sectional view of a conventional vertical MOS transistor having a trench structure. A semiconductor substrate is prepared in which a lightly doped layer 2 of a first conductive (or conductivity) type is epitaxially grown on a heavily doped substrate 1 of

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